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A New Control Scheme of Class-E Electronic Ballast with Low Crest Factor

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ABSTRACT

In this paper, a new control scheme of Class-E inverter for reducing the crest factor of electronic ballasts for fluorescent lamps using Pulse-Frequency-Modulation (PFM) is introduced The lifetime of the lamps is guaranteed by decreasing the lamp crest factor and also voltage stress of the switch is significantly decreased by a new scheme although conventional Class-E inverter is used in this paper. The proposed PFM control scheme didn't use any auxiliary circuit. The proposed control strategy is executed by feeding back the input voltage, and the zero-voltage-switching (ZVS) is ensured by maintaining constant turn-off time of the switch Therefore, the control principles of proposed method are explained in detail and its validity is verified through several simulations and experimental results.

Keywords: Class-E inverter, Electronic Ballast, Crest Factor, Pulse-Frequency-Modulation (PFM), Zero-Voltage-Switching (ZVS)

1. Introduction

Recently, with remarkable progress of the power semiconductor device, much attention has been focused the high frequency of the ballast for fluorescent lamp. The fluorescent lamp provides a large percentage of lighting needs because its higher luminous efficacy (lm/w), which is the energy conversion efficiency of the lamp. However, the size of fluorescent lamp is considerably larger than incandescent lamp because it needs a large fixture and ballast Electronic ballast is required for the fluorescent lamp or gaseous discharge lamps since these have negative resistance characteristics in the desired region of operation[1-8] These characteristics make an unstable condition of the lamp So, the electronic ballast must provide a sufficiently a higher starting voltage, a current limiting after starting Also, high crest factor of the lamp current reduces the lifetime of the lamp as well as luminous efficiency The electronic ballast meets the traditional accepted limit of crest factor 2 1 However, the lifetime of the lamp is not guaranteed by above mentioned condition As a result, crest factor value should be required below 1 7 to assure its lifetime, in these days[5]

Recently, for low cost electronic ballast applications, single-stage schemes were preferred The single–stage ballast topologies, Class-E inverter has drawn much attention because of its simplicity and inherent soft switching feature[1][2]

The Class-E inverter in ballast applications for

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fluorescent lamps presents advantages such as: high efficiency, simplicity, lightweight, high frequency operation and sinusoidal output Also, if the lamp is operated in very high frequency (in the range of MHz), it is possible to substitute the electrodes of the lamp by capacitance. All these characteristics make them very adequate to handle fluorescent lamps[1-10]

However, the conventional Class-E electronic ballast has some drawbacks such as high crest factor of the lamp current In addition, it has some drawbacks such as the reduced switch utilization ratio because of the voltage stress of switch by resonance during turn-off time and the increased conduction loss in Class-E electronic ballast Therefore, conventional Class-E inverter is difficult to make an electronic ballast of low cost.

Recently, Class-E inverter of the various kinds was proposed to solve these problems[14]. It is applied to the inverter for electronic ballast due to the reduced voltage stress by clamping the main switch voltage compared with Class-E inverter. Also, the Hybrid-ACCE inverter has good characteristics, which are the switching loss and EMI of overall system due to the reduced switching of the auxiliary switch. However, in spite of these characteristics, this Class-E inverter has disadvantages of high crest factors or high cost system due to the additional auxiliary circuit.

Therefore, the Class-E electronic ballast with a new control scheme is proposed to solve these problems In this paper, the proposed control scheme is achieved by variable switching frequency through the feedback of the input voltage High crest factor of electronic ballast for fluorescent lamps can be reduced by the proposed new control scheme (PFM) In addition, the voltage stress of the switch can be reduced by variable frequency The new Class-E electronic ballast for the fluorescent lamp has the advantages of not only good performance of conventional Class-E electronic ballast but also a low cost system due to the reduction of voltage stress of the switch Also, the switching loss of the Class-E inverter is reduced because Zero-Voltage-Switching (ZVS) of the switch is accomplished at turn-on The operation principle of the characteristics of electronic ballast with the proposed PFM control scheme is described in detail, and its validity is verified through simulation and experimental results.

2. Circuit Description

Fig 1 shows the overall Class-E inverter system for electronic ballasts

It consists of the rectifier bridge diode on the part of the input, small filters, L_f, and, C_f, the current shape inductor, L_1, switch, S, parallel capacitor, C_p, blocking capacitor, C_b, resonant inductor, L_r, resonant capacitor, C_r, start-up capacitor, C_s, and lamp equivalent resistor, R[11]

2.1 The Principles of Operation

The Class-E inverter for the electronic ballast operates identically in comparison with a conventional Class-E inverter. Turn-off time of switch should be constantly maintained to achieve ZVS of the switch, and achieving ZVS at turn-on reduces thus switching loss. Also, the switching losses are reduced due to resonance between current shaper inductor, L_1, and parallel capacitor, C_p, at turn-off As a result, the switch of the inverter system has nearly zero-switching loss, which means high efficiency[12][13]. To analyze operating modes of the Class-E electronic ballast system with the proposed control scheme, we make the following assumptions.

- All components are ideal.
- Input voltage of DC link is constant in one switching cycle.
- Electronic ballast operates in its steady state.

Operating principles of the Class-E electronic ballast with the proposed PFM control scheme are explained in detail when it is applied to the lamp

Fig 2 shows theoretical waveforms and Fig.3 shows operational modes of the Class-E inverter.

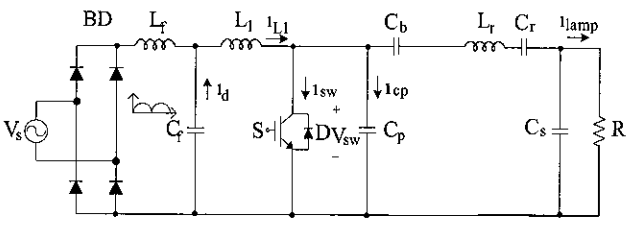


Fig 1 The overall Class-E inverter system for Electronic Ballasts.

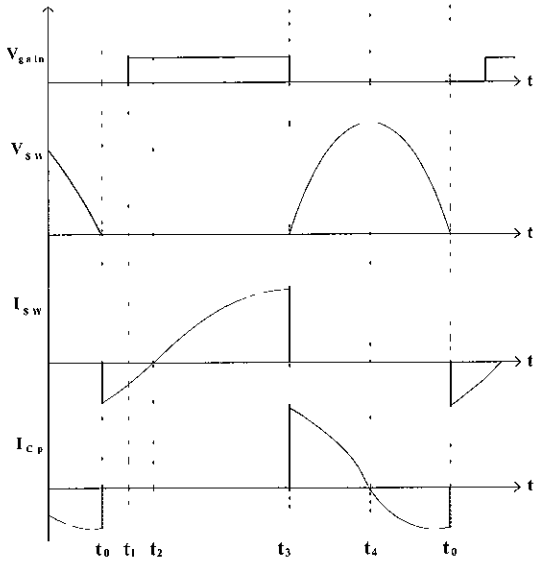
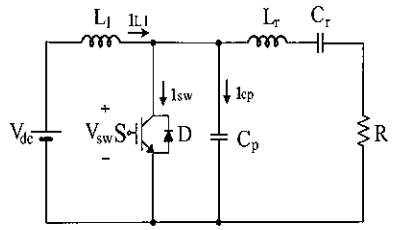
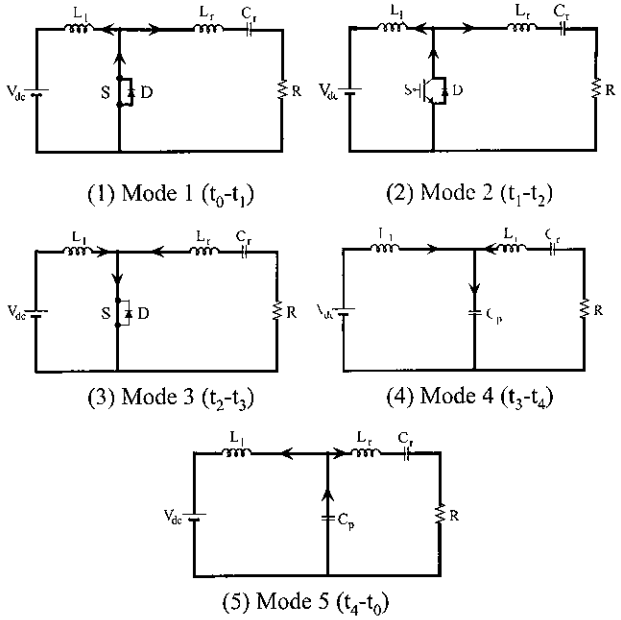


Fig 2 Theoretical waveforms of the Class-E inverter mode



(a) Equivalent circuit of the proposed Class-E electronic ballast



(b) Operational modes of the Class-E electronic ballast

Fig. 3 Equivalent circuit and operational modes of the Class-E inverter.

2.1 1 Turn-on state of the switch Stage 1 (Mode1, Mode 2, Mode 3)

The anti-parallel diode of switch, D, is conducted at t_0, and at this time, the ZVS condition of the switch, S, can be satisfied The load current, i_{lamp}, flows through anti-parallel diode of switch, and switch, S, is turned on under ZVS condition at t_1 In this stage the supply current i_{L1} and i_{lamp} pass through switch The switch voltage and current equations of the equivalent circuit are represented by Eq. 1 and Eq. 2 during this stage

$$-V_{dc} + L_1 \frac{di_{L1}}{dt_{(on)}} = 0,$$

$$-L_1 \frac{di_{L1}}{dt_{(on)}} + \frac{1}{C_r}\int i_{cr}dt + R_{lamp} i_{lamp} = 0 \qquad (1)$$

$$i_{sw} = i_{L1} + i_{lamp} = I_{L1}(t_{on}) + \frac{V_{dc}}{L_1}(t - t_{on}) + I_{lamp}\sin(\omega t + \varphi) \qquad (2)$$

where, $\omega=2\pi f_S$, f_S: the switching frequency, φ: the load angle.

2 1.2 Turn-off state of the switch Stage 2 (Mode 4, Mode 5):

When switch, S, is turned off at t_3. Switch voltage, V_{sw}, is increased at mode 4, and then the switch voltage is decreased by turned over of the load current at mode 5 The supply current, i_L, and the output current, i_{lamp}, passes through C_p The voltage and current of parallel capacitor, C_p, equations of the equivalent circuit are represented by Eq 3 and Eq. 4 at turn-off.

$$-V_{dc} + L_1 \frac{di_{L1}}{dt} + \frac{1}{C_p}\int i_{cp}dt_{\_off} = 0 \qquad (3)$$

$$L_r \frac{di_{Lr}}{dt} + \frac{1}{C_r}\int i_{cr}dt_{\_off} + \frac{1}{C_p}\int i_{cp}dt_{\_off} + R_{lamp} i_{lamp} = 0$$

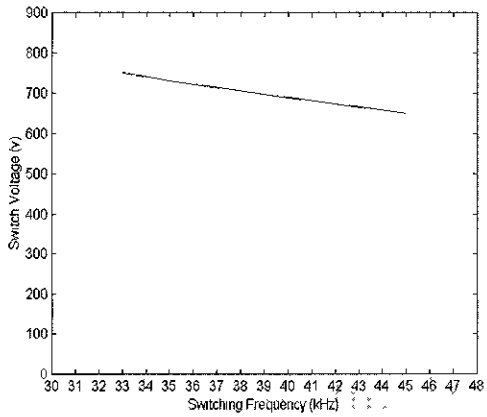
$$i_{cp} = i_{L1} + i_{lamp} = C_p \frac{dv_{cp}}{dt} + I_{lamp}\sin(\omega t + \varphi) + I_{lamp}\sin(\omega t + \varphi) \qquad (4)$$

3. Analysis of Class-E Inverter System

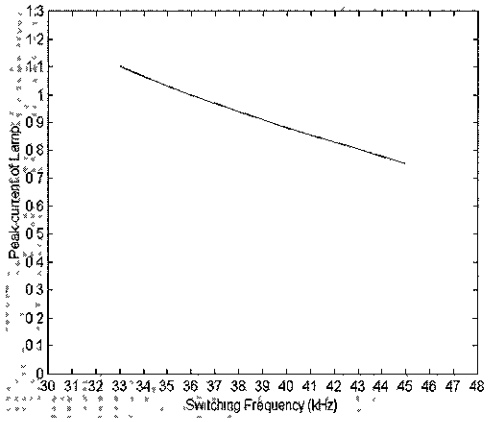
Fig. 4 shows the relation between switch voltage & current and switching frequency by condition of input voltage and switching frequency Fig 4(a), (b) and (c), (d) are plotted by the result of Eq. 2 and Eq. 3. At this time, resonant time, t_{off}, is assumed constantly.

Fig 4(a) and (b) shown that the input voltage is fixed and switching frequency is variable As known by Fig. 4(a), switching frequency is changed from 33 kHz to 45 kHz due to avoid acoustic noise and switch voltage acquires 650V As seen by Fig. 4(b), Peak current of lamp is variable to 0 75A. As known in Fig 4(a) and 4(b), switch voltage and lamp current are decreased by the increased switching frequency because switch voltage is in inverse proportion to switching frequency, as mentioned Eq. 2 and Eq. 3.

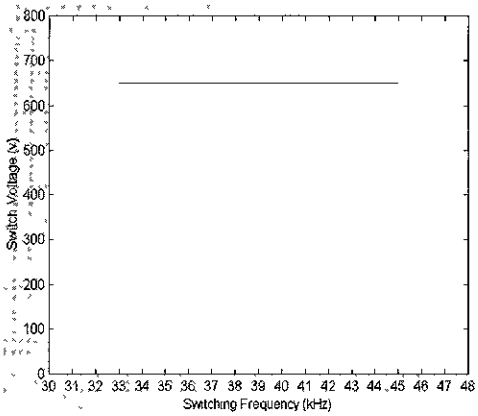
Fig. 4(c) and (d) show that input voltage is changed by 120Hz ripple components and switching frequency is changed from 33 kHz to 45 kHz As known in Fig 4(c) and (d), switch voltage and peak current of lamp is clamped constantly if input voltage and switching frequency are changed at the same time. As known in these results, the clamping level of lamp current is decided by switching frequency Switching frequency is in inverse proportion to clamping level. Therefore, high crest factor of electronic ballast for fluorescent lamps can be reduced by the proposed new control scheme (PFM). In addition, the voltage stress of the switch can be reduced by variable frequency.



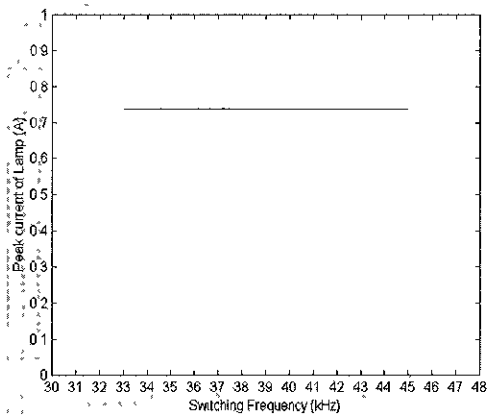
V_{sw}, variable f_s
(a)



i_{lamp}, variable f_s
(b)



V_{sw}, variable f_s
(c)



i_{lamp}, variable f_s
(d)

Fig 4 The relation between switch voltage & current and switching frequency by condition of input voltage and switching frequency

4. The Proposed New Method Principle for Reduction of Crest Factor

4.1 Definition of Crest Factor

The crest factor (CF) is defined as,

$$CF = \frac{I_{lamp,peak}}{I_{lamp,rms}} \tag{5}$$

It is related with the lifetime of the lamp. The crest factor less than 1.7 results in the maximum long life expectancy[4]. If the ripple of the lamp current envelope becomes smaller, the crest factor will be reduced. The crest factor is considerably related to the lamp lifetime. So, if peak current of lamp is reduced, the crest factor is reduced as known by Eq. 5.

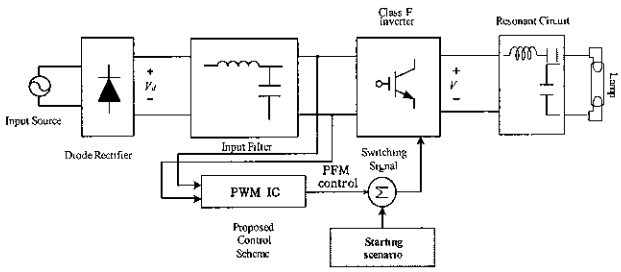
4.2 Pulse Frequency Modulation (PFM)

In this paper, the Class-E inverter with the proposed PFM scheme can clamp lamp current without the any auxiliary circuit. In addition, it can decrease voltage stress of switch through modulation of switching frequency. As a result, the crest factor and the rated voltage of switch can be reduced by clamping the lamp peak current. Also, the output power of the Class-E inverter with the PFM scheme is the same as the conventional Class-E inverter, since Class-E inverter with PFM scheme acts as the conventional Class-E inverter at below clamping level. The overall block diagram and of the proposed control scheme is shown in Fig. 5(a). The proposed simple control scheme consists of one-control loop and its control loop modulates switching frequency.

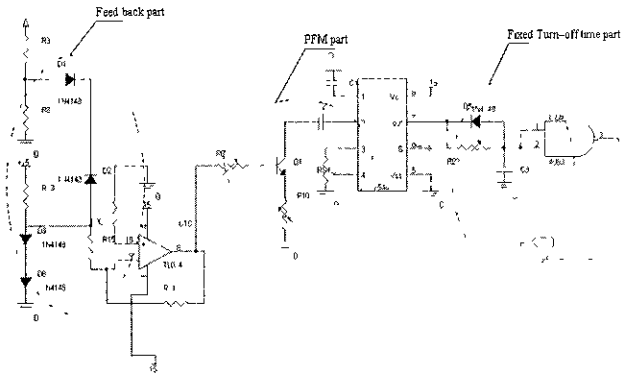
Fig. 5(b) shows the implemented control circuit to execute the proposed control scheme. The proposed control circuit consists of three control parts. Among them, feedback part feeds back the input voltage and compares it with the clamping level. As a result, clamping level of the inverter system is calculated by the input voltage. Next, the calculated value is added on the PFM part and the switching frequency is modulated by PFM part. Lastly, the turn-off time of the changed switching frequency does not stay constant. In this case, ZVS of the switch cannot be achieved. So, turn-off time of the switch must be constantly maintained to get ZVS of the switch. The fixed turn-off time part guarantees the regular turn-off time to assist the resonance between the L_1 and C_p. Therefore, the proposed control scheme makes the constant turn-off time and the changed switching frequency according to the input voltage as well as crest factor of the lamp and the voltage stress of the switch is significantly reduced.

Fig. 6 shows the control principle of the proposed PFM.

As known in Fig. 6(a), the PFM control scheme decides whether switching frequency is modulated or not by input voltage. Therefore, according to the input voltage, v_d, the proposed PFM scheme to reduce the crest factor and to clamp switch voltage using class-E inverter is explained through experimental results as followings. In case that input voltage increases, the lamp current, i_{lamp}, is clamped any constant level by increasing switching frequency. First, when the system with the proposed control scheme operates at constant switching frequency, f_{s1}, like the conventional Class-E inverter, the lamp current, i_{lamp}, goes up in proportion to the input voltage as known. As input voltage reaches, V_1, the lamp current, i_{lamp}, is arrived at

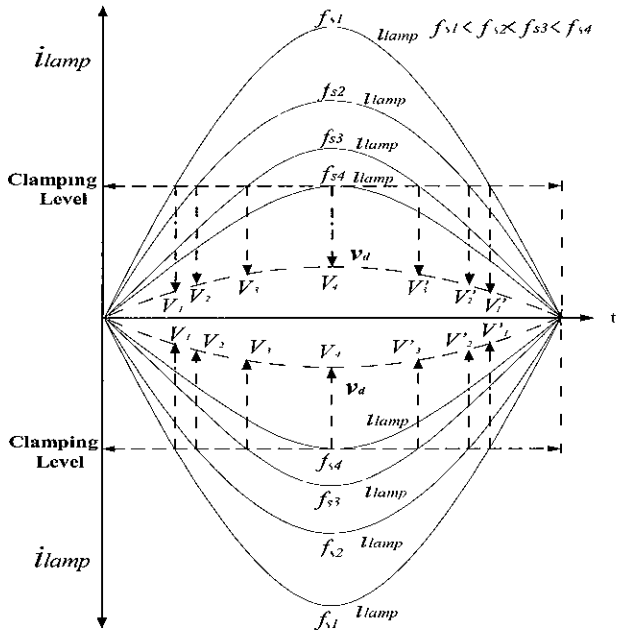


(a) Block diagram

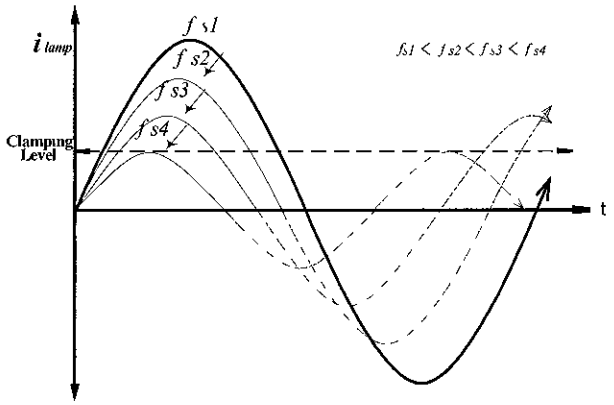


(b) Control circuit

Fig. 5 Block diagram & Control circuit of Class-E electronic ballast system with new control scheme



(a) Switching frequency vs lamp current with clamping level in one switching cycle



(b) Modulation of the switching frequency vs peak current of lamp with clamping level in one switching cycle

Fig 6 The control principle of the proposed PFM

clamping level After that, in case that input voltage is larger than V_1, the switching frequency should be increased so that the lamp current, i_{lamp}, is constantly maintained at clamping level That is to say, as input voltage goes up from V_1 to V_2, V_2 to V_3, the switching frequency is increased from $f_{s1}$to f_{s2}, f_{s2} to f_{s3} respectively. Subsequently, as input voltage reaches the maximum voltage, V_4, the switch voltage can be kept at clamping level constantly by increasing the switching frequency to f_{s4}. As input voltage is reduced after one half cycle, $V_4 \rightarrow V_3' \rightarrow V_2' \rightarrow V_1'$, the switching frequency is also decreased, $f_{s4} \rightarrow f_{s3} \rightarrow f_{s2} \rightarrow f_{s1}$ Then, the Class-E inverter with PFM control scheme acts as a conventional Class-E inverter by operating constant switching frequency, f_{s1}, repeatedly when input voltage is lower than V_1

As shown in Fig 6(a), the lamp current is clamped by the proposed control scheme as a constant level in spite of the change of input voltage, v_d, switching frequency, f_{s1}, repeatedly when input voltage is lower than V_1 As shown in Fig 6(a), the lamp current is clamped to a constant level by the proposed control scheme Then, the control principles of the opposite waveform are the same as above explained

Fig 6 (b) shows the modulation of the switching frequency vs the peak current of lamp with clamping level in one switching cycle As known in Fig 6(b), peak current of lamp is clamped, as switching frequency is increased from f_{s1} to f_{s4} with closed loop during one cycle of lamp current Inverter system with the proposed PFM method acts as the constant switching frequency at below clamping level of lamp current, and acts as variable switching frequency at over clamping level of lamp current according to the magnitude of the feed back input voltage.

As a result, the peak current and crest factor of the lamp is significantly reduced as shown in Fig. 6 So, the proposed control scheme guarantees the life of the lamp

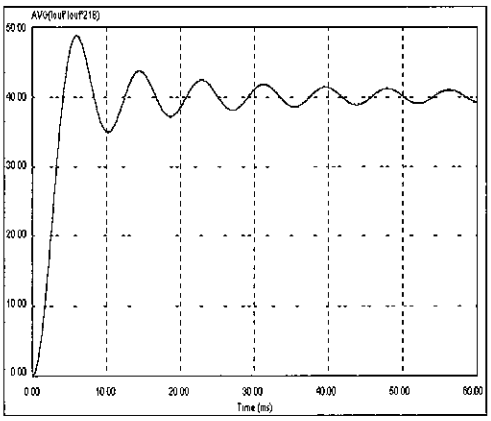
5. Simulation and Experimental Results

To verify the validity of the Class-E inverter system with the proposed control scheme, the experiment was performed under the same circuit and parameters in Table 1 The simulation and experiment were performed under the same power with and without the proposed control scheme using the conventional Class-E inverter. Here, switching frequency of the Class-E inverter with the proposed control scheme is changed from 33 kHz to 45 kHz so that inverter avoids acoustic noise and switch voltage acquires 650V as mentioned above.

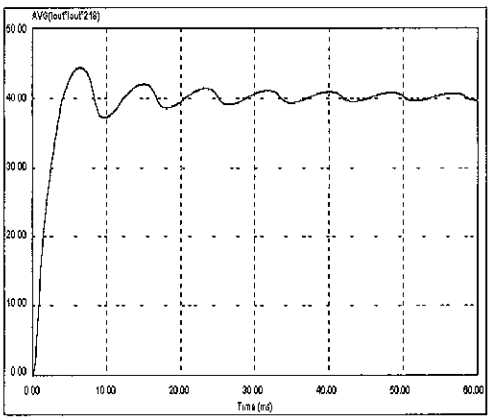
Fig 7(a) and (b) show the output power of the conventional Class-E inverter and the Class-E inverter with proposed control scheme respectively

Table 1 Utilized parameters for experiment of the proposed Class-E inverter with PFM control scheme

COMPONENTS		PARAMETERS
V_s	Input voltage	110Vac / 60Hz
f_s	Switching frequency	33kHz ~ 45kHz
f_r	Resonant frequency	46kHz
L_f	Input filter	1mH
C_f	Input filter	1uF
L_r	Resonant inductor	4.3mH
R_{lamp}	Equivalent lamp resistor	218Ω
C_r	Resonant capacitor	100nF
C_p	Parallel capacitor	40nF
C_b	Blocking capacitor	100uF
Cs	Start-up capacitor	5nF
L_1	Current shape inductor	0.35mH
S	Switch	IGBT F 90N60UFD



(a) The output power of conventional inverter



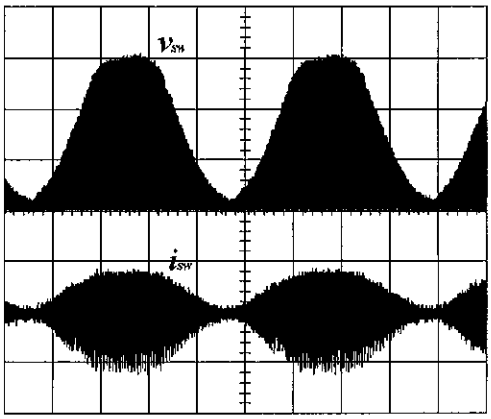
(b) The output power of Class-E inverter Class-E with PFM control system

Fig 7 The simulated results of average output power.

From these waveforms, the conventional Class-E inverter and the Class-E inverter using proposed control scheme is confirmed to equal output power about 40W.

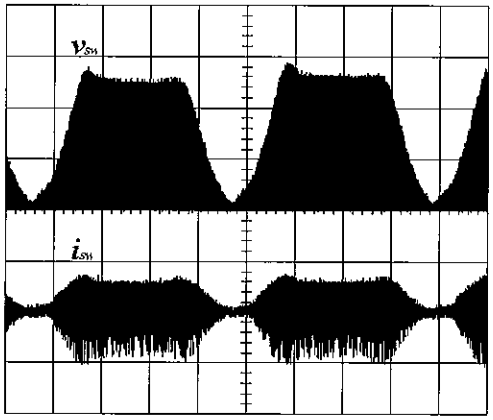
Fig. 8 shows the switch voltage, V_{sw}, and the switch current, i_{sw}, of conventional Class-E inverter without PFM in case that the system is operated at constant switching frequency, 40 kHz. In this case, the peak current of the switch was measured about 4A and the switch voltage, V_{sw}, is increased by 4.8 (Quality Factor) Therefore, it is shown that conventional Class-E inverter has the peak voltage of the switch, which is about 750V.

Fig. 9 shows the switch voltage, V_{sw}, and the switch current, i_{sw}, of the Class-E inverter with the proposed PFM control scheme in case that switching frequency is continuously modulated from 33 kHz to 45 kHz In this case, the peak current of switch was measured about 3A The peak voltage of switch is measured about 650V As shown in Fig 9, the switch voltage is considerably reduced due to the proposed control scheme being implemented. If Class-E inverter with the PFM scheme does not implement the PFM control, the switch voltage is increased as high as switch voltage of the conventional Class-E inverter. Also, it is verified from Fig 9 that the switch current is reduced, so it means power to be constant while switch voltage is increased. It is very interesting feature of the class-E inverter using the proposed PFM method in this paper.



(250V/div , 5A/div , time 2ms)
V_{sw}, i_{sw}

Fig 8 The experimental results of the conventional Class-E inverter without PFM.



(250V/div , 5A/div , time 2ms)
V_{sw}, i_{sw}

Fig 9 The experimental results of the Class-E inverter with PFM

As known seen from the Fig. 8 and the Fig. 9, a new control method using proposed PFM is confirmed that the peak current of the switch and voltage stress of switch can be significantly reduced

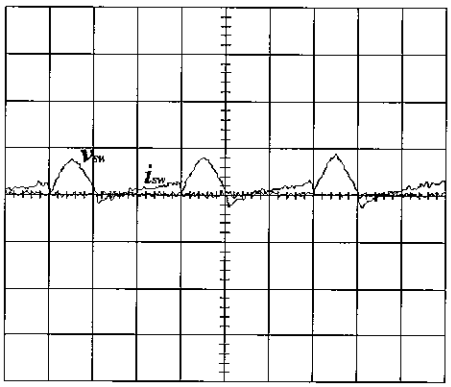
Fig 10 shows the voltage and current of the switch of the Class-E inverter with the proposed PFM control scheme

Fig. 10(a) shows waveforms of the switch voltage and current when 33 kHz. As seen in these waveforms, it can be found the Class-E inverter is operated by low frequency when the input voltage is lower than clamping voltage level of the switch, and also ZVS of the switch is safely achieved at turn-on

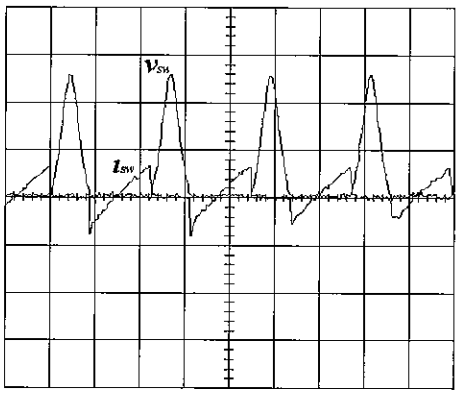
Fig. 10(b) shows waveforms of the switch voltage and current when the input voltage attains to its maximum voltage of over clamping level, the switching frequency is continuously changed by 45 kHz. From these waveforms, we know that the switch current and switch voltage is continuously clamped at the same level as the Class-E inverter operated with constant frequency control. Also, in spite of the switching frequency being varied, the ZVS of the switch can be achieved stably

As known seen from the Fig 10(a) and the Fig. 10(b), a new control method using proposed PFM is confirmed that the ZVS of the switch can be achieved

Fig. 11 shows the experimental results of the lamp current of the conventional Class-E inverter and the Class-E inverter system with the proposed PFM control



(250V/div , 5A/div , time· 10us)
(a) V_{sw}, i_{sw} (At below clamping level)

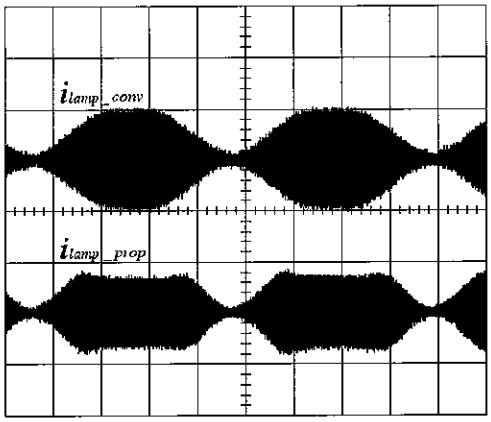


(250V/div , 5A/div , time 10us)
(b) V_{sw}, i_{sw} (At over clamping level)

Fig 10 The experimental results of the Class-E inverter system with the proposed PFM control scheme.

scheme Upper trace of Fig 11 is the lamp current of the conventional Class-E inverter and under trace of Fig 11 is the lamp current of the Class-E inverter system with the proposed PFM control scheme

As shown in Fig 11, the peak current lamp of conventional Class-E inverter was measured about 1A In this case, it is shown that conventional Class-E inverter has the crest factor, which is about 1.9 Also, the peak current lamp of the Class-E inverter system with the proposed PFM control scheme was measured about 0 75A In this case, the crest factor of the Class-E inverter with the proposed control scheme is measured about 1.58 Therefore, Fig 11 is shown that the peak current of the Class-E inverter system with the proposed PFM control scheme lower than the peak current of conventional method.



(1A/div , time 2ms)

i_{lamp}

Fig 11 The experimental results of conventional Class-E inverter and the Class-E inverter system with the proposed PFM control scheme

Eventually, it is considerably less than conventional crest factor 1.7 as well as is very interesting feature of this work.

As a result, a new control method using PFM is confirmed that the crest factor of lamp current and voltage stress of switch is reduced through experimental results.

Therefore, we know that the above experimental results are good agreement with the theoretical analysis in the section IV

6. Conclusion

In this paper, the operation of the electronic ballast for fluorescent lamps is considered in detail, and a new control method using PFM for reducing crest factor is proposed Also, the feasibilities of the class-E electronic ballast with the proposed control scheme are verified through the experimental results. From these results, the feasibilities of the Class-E electronic ballast with the proposed control scheme are the same as the followings

Reduction of the crest factor by the proposed Class-E electronic ballast using PFM

- Reduction of the voltage stress of the switch by varying switching frequency
- Low cost system because the rating voltage of the switch is reduced by suppressing the voltage
- The stable ZVS of the switch

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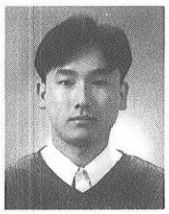

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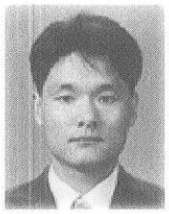

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